In the United States Patent and Trademark Office

In re the application of: Fleming Andersen		
Filed: 10/05/2000	Group Art Unit:	2121
For: Fully Exhibiting Asynchronous Behavior in a Logic Network Simulation	Examiner:	Thomas K. Pham
Appl. No.: 09/679,780		
Applicant's Docket: AUS920000494US1		

Attention: Official Draftsperson
US Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

IN THE DRAWINGS

Formal Drawings are herein submitted as requested in the Office Action.

Respectfully submitted,

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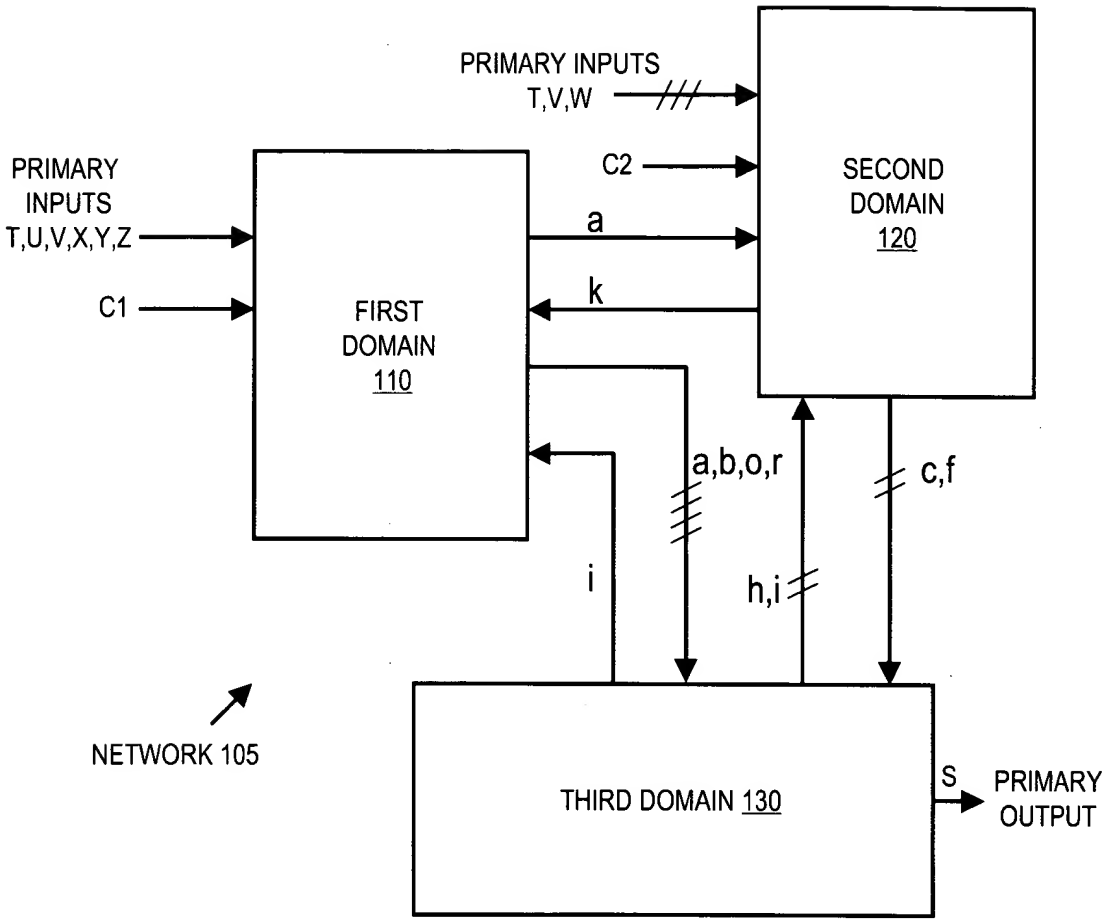

FIG. 1

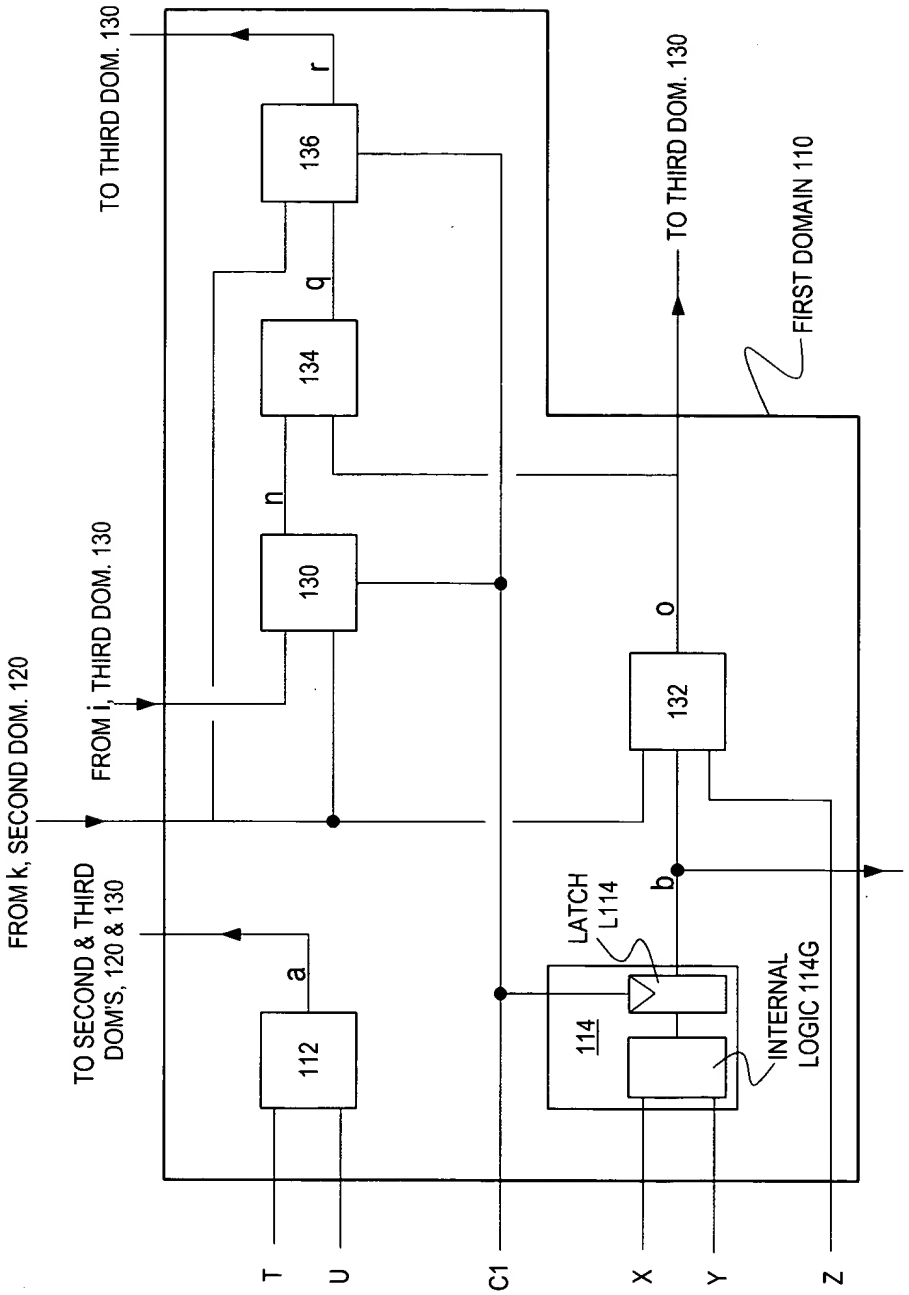

FIG. 2

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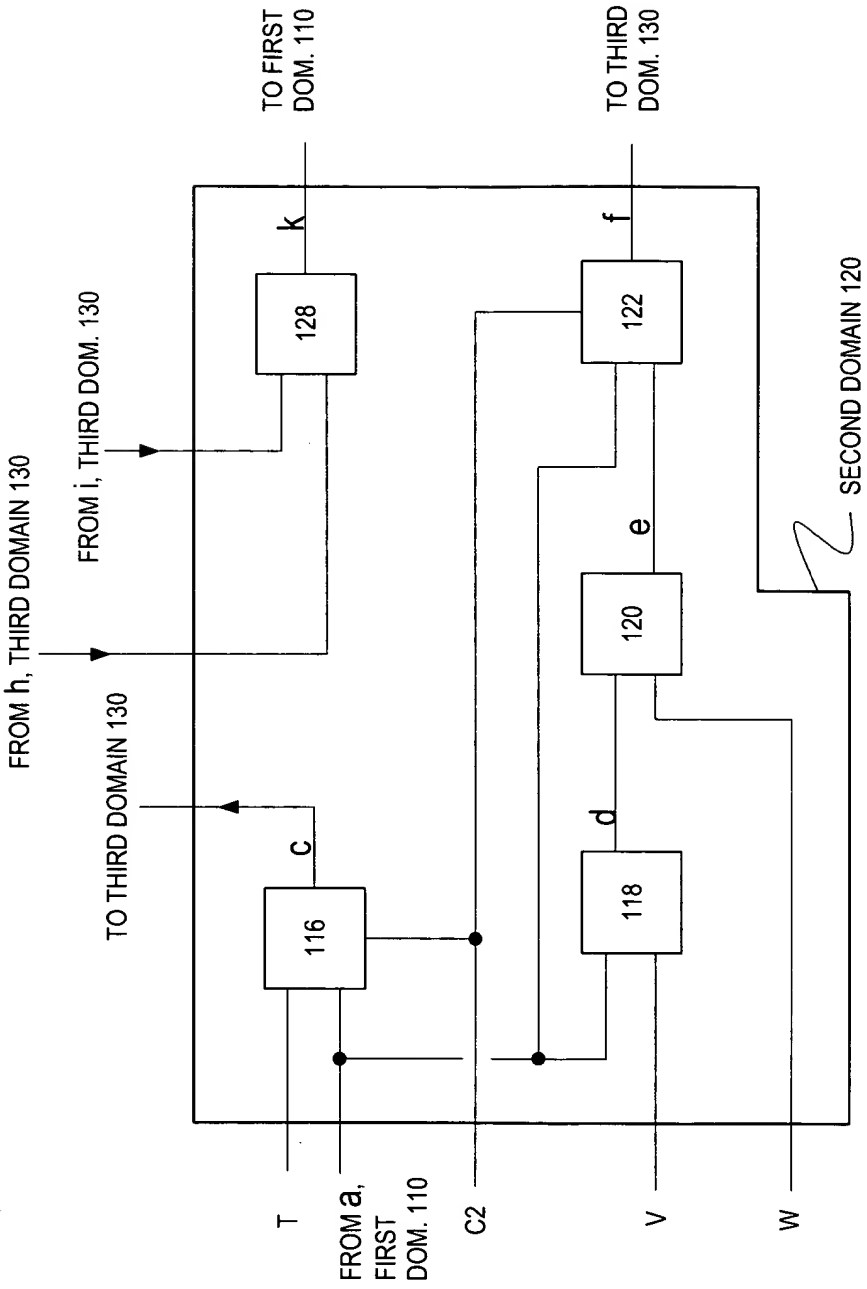

FIG 3

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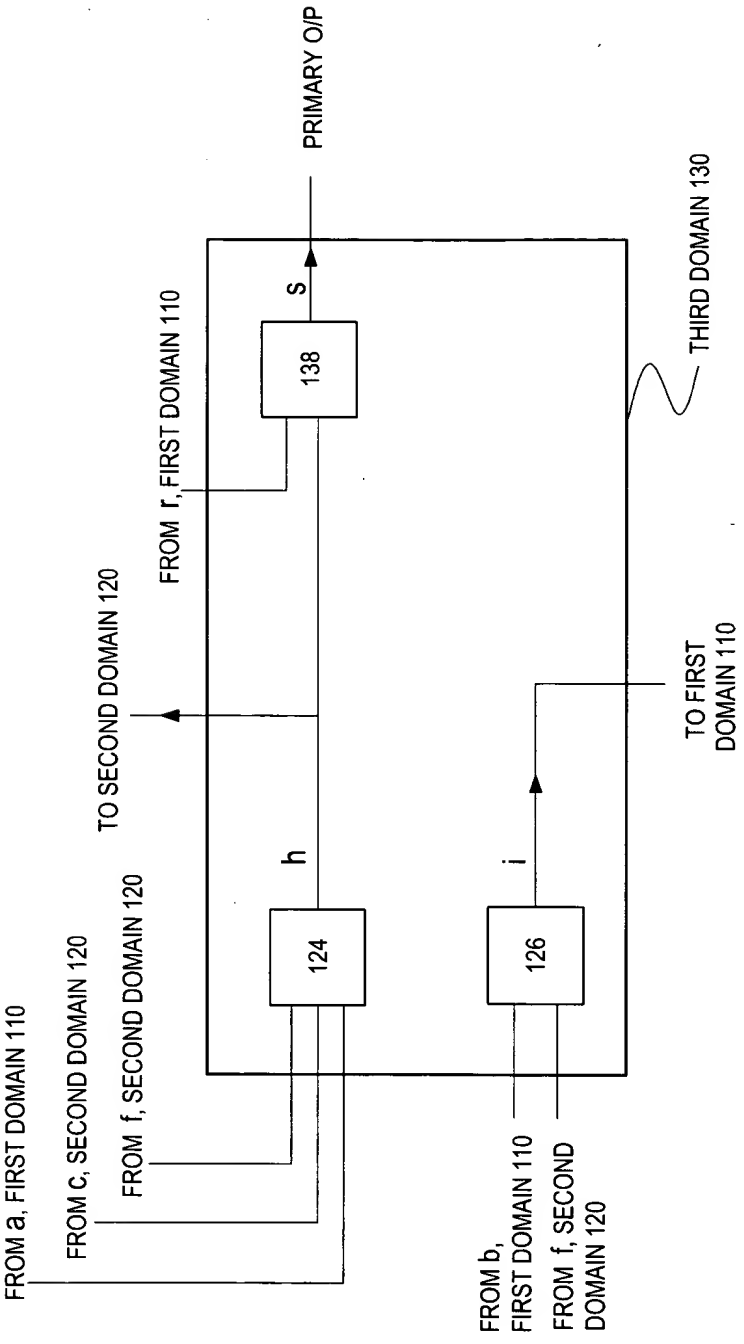

FIG 4

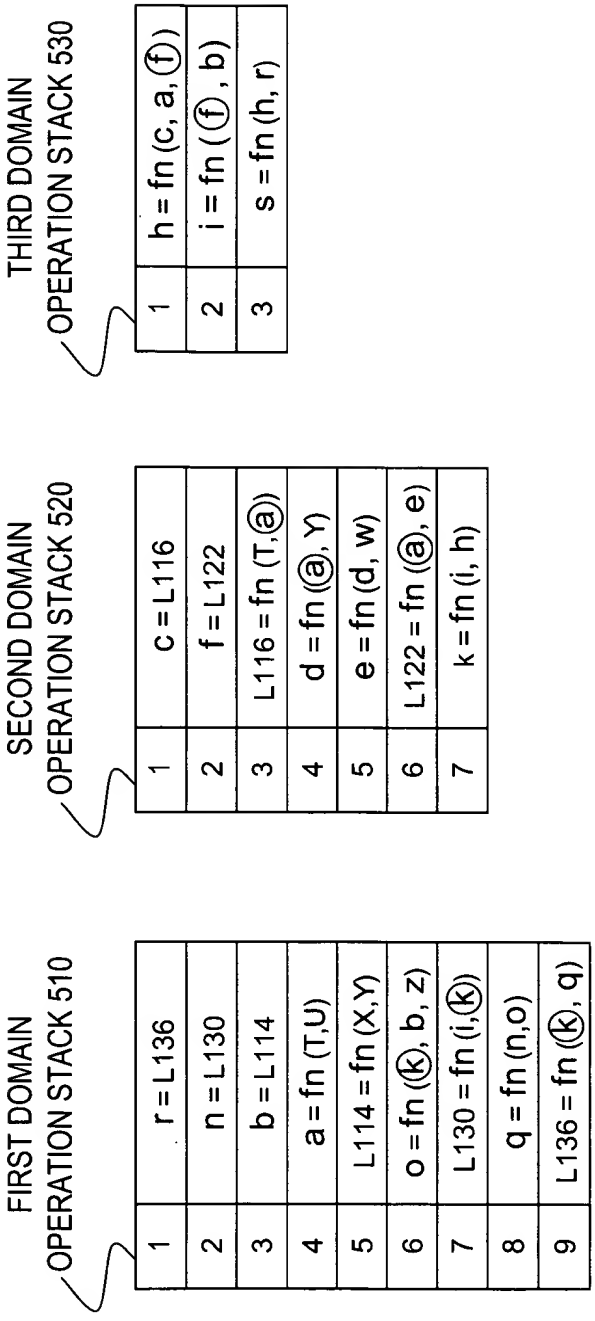

FIG. 5

FIRST DOMAIN OPERATION STACK 610

1	r
2	n
3	b
4	a
5	L114
6	o
7	--
8	--
10	--
11	--
12	--
13	--
14	L130
15	q
16	--
17	--
18	--
19	--
20	--
21	--
22	L136

SECOND DOMAIN OPERATION STACK 620

1	c
2	f
3	L116
4	--
5	--
6	--
7	--
8	--
9	--
10	--
11	--
12	--
13	d
14	e
15	--
16	--
17	--
18	--
19	--
20	--
21	--
22	--
23	L122
24	k

THIRD DOMAIN OPERATION STACK 630

1	h
2	--
3	--
4	--
5	--
6	--
7	--
8	--
9	i
10	s

FIG. 6

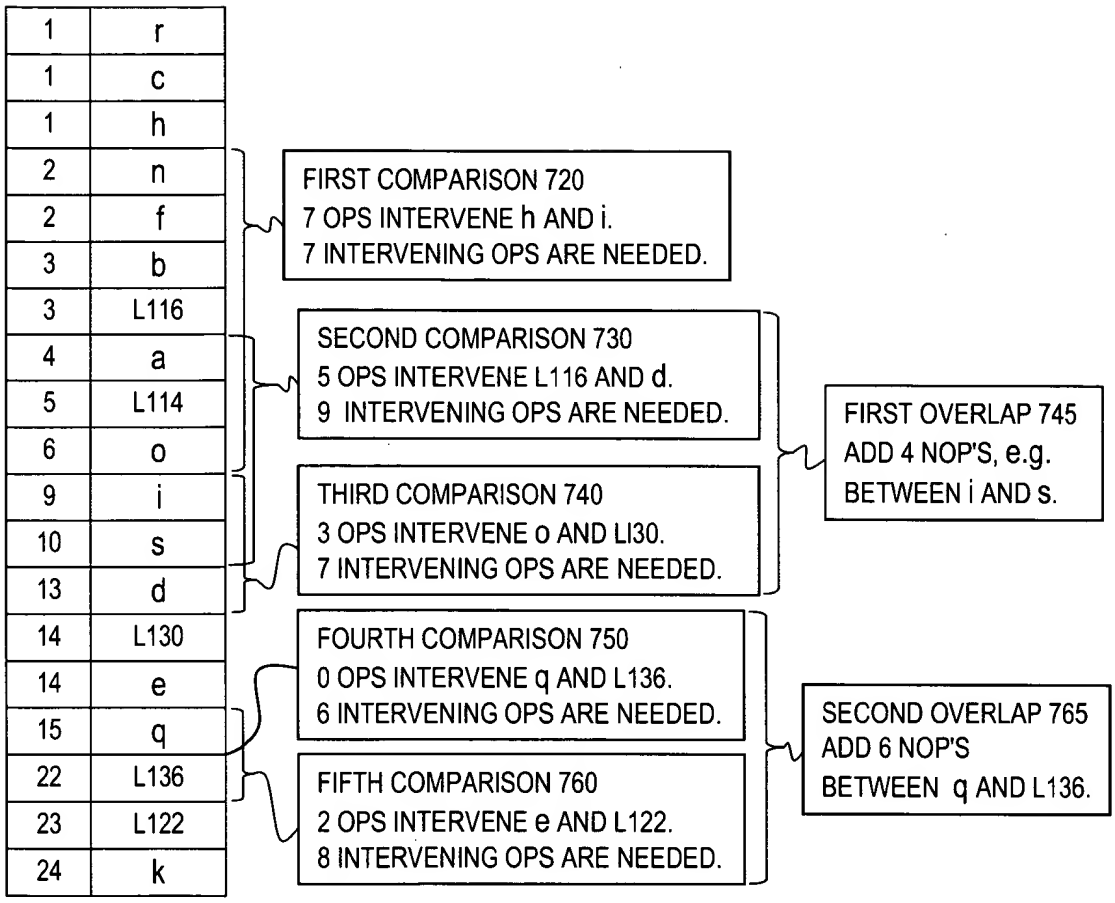

FIG. 7

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MERGED OPERATION STACK 810

1	r
2	c
3	h
4	n
5	f
6	b
7	L116
8	a
9	L114
10	o
11	i
12	--
13	--
14	--
15	--
16	s
17	d
18	L130
19	e
20	q
21	--
22	--
23	--
24	--
25	--
26	--
27	L136
28	L122
29	k

FIG. 8

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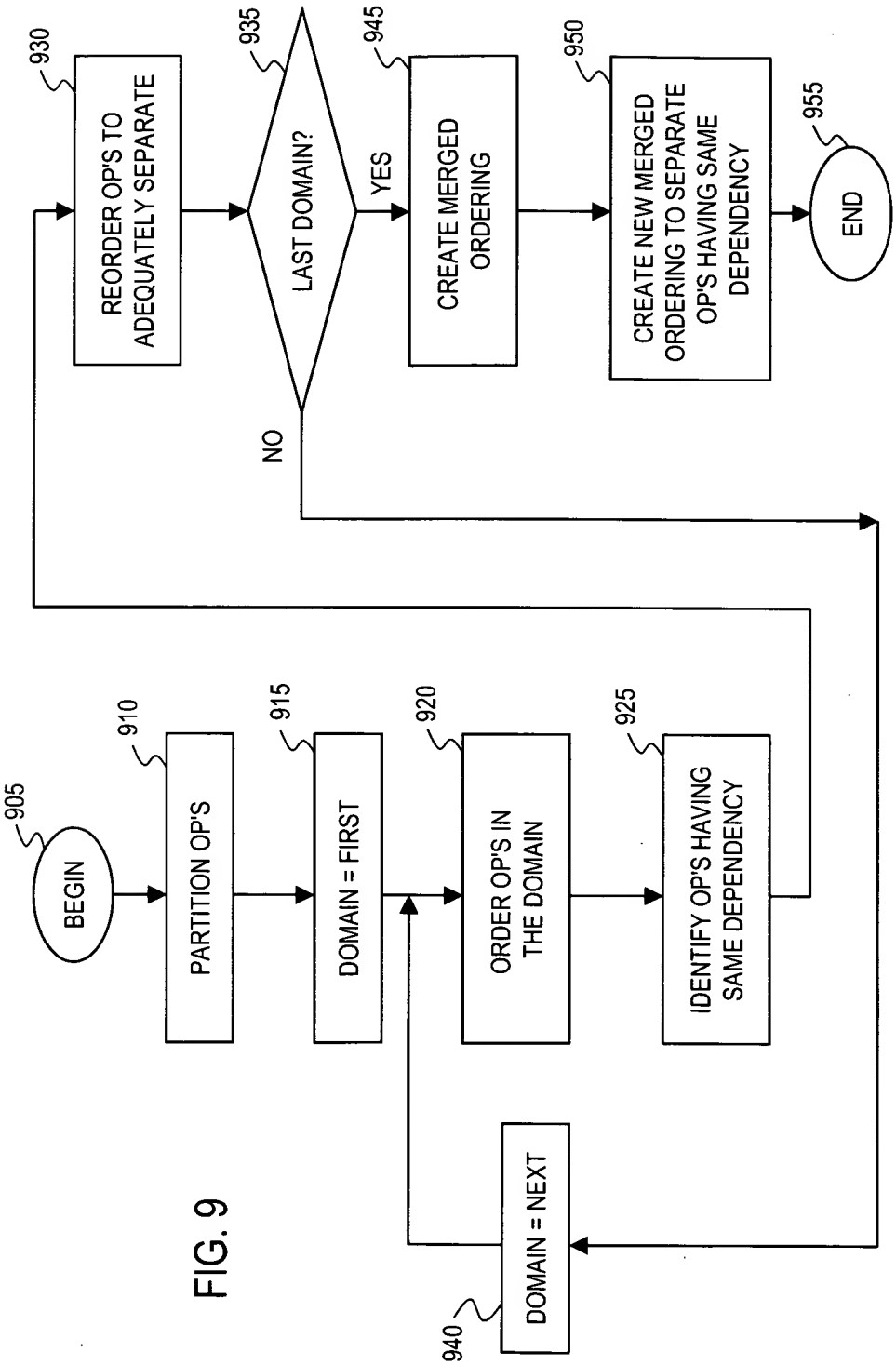

FIG. 9

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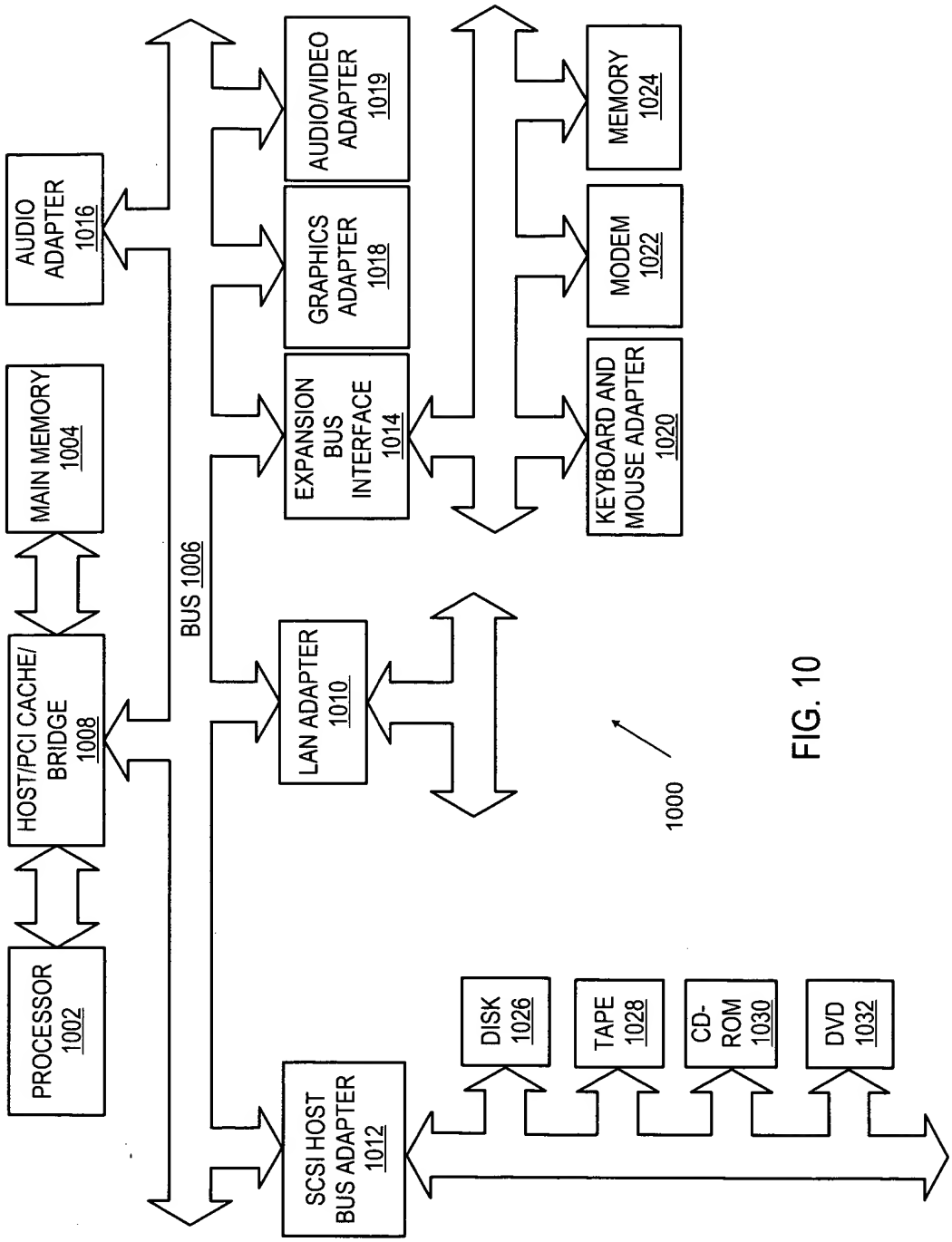

FIG. 10